



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,563	02/23/2002	Masahiro Ishida	ADV A225.001AUS	3180

7590 11/02/2006
MURAMATSU & ASSOCIATES
114 PACIFICA SUITE 310
IRVINE, CA 92618

EXAMINER

GHULAMALI, QUTBUDDIN

ART UNIT	PAPER NUMBER
----------	--------------

2611

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.

10/082.563

Applicant(s)

ISHIDA ET AL.

Examiner

Qutub Ghulamali

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 8/9/2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 13, 14, 17-24, 32 and 34-37 is/are rejected.
- 7) ☒ Claim(s) 9-12, 15, 16, 25-31 and 33 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This Office Action is responsive to applicant's Remarks/Amendments filed on 08/09/2006.

Response to Remarks/Amendment

2. The applicant's remarks/amendment, filed 08/09/2006, with respect to claims 1, 17, 34 and 36, under 35 U.S.C. 102(e), have been fully considered but are moot in view of the new ground(s) of rejection. The rejection based on new art follows:

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 5, 6, 8, 17-18, 21-24, 34, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al (USP 6,661,860) in view of Dalal et al (USP 6,661,836).

Regarding claims 1, 17, 34, 36, Gutnik discloses a probability estimating apparatus (jitter estimation system and related techniques) for peak-to-peak values in clock skews (jitter) among a plurality of clock signals comprising:

Art Unit: 2611

a clock skew estimator (jitter estimation) for estimating clock skew sequences among the plurality of clock signals (SigA and SigB) under test (abstract; col. 5, lines 17-40; col. 6, lines 50-66). Gutnik however, does not explicitly disclose a probability estimator for determining a generation probability of the peak-to-peak values in the clock skews among the plurality of clock signals under test based on the clock skew sequences from the clock skew estimator by applying Rayleigh distribution. Dalal in a similar field of endeavor discloses a probability estimator (creates a histogram that represents the probability density function of signal edge placement) for determining a generation probability of the peak-to-peak values in the clock skews among the plurality of signals (multiple repetitions of the signal) under test based on the clock skew sequences from the clock skew estimator (col. 2, lines 32-41; col. 3, lines 52-67; col. 4, lines 13-30; col. 5, lines 51-67). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use statistical estimation of applying Gaussian or Rayleigh distribution as taught by Dalal in the system of Gutnik because such estimation can provide instantaneous signal skew among interfering signal under test due to shift in frequency. The examiner notes that in the context of instant claims, signal fading as normally applied with mobile communication, is purely analytical and that Rayleigh distribution is well known in the art and applied to signals Gaussian in nature as noted in the attached Text reference, pages 127-128; to Edward A. Lee and David G. Messerschmitt, as applied for estimating skew or deviation to estimates derived in Dalal.

Regarding claims 2 and 18, Gutnik discloses probability estimator determines the generation probability of a peak value of the clock skews among the plurality of signals under test based on said clock skew sequences (col. 10, lines 33-44).

Regarding claim 6, Gutnik discloses clock skew estimator includes a second clock skew calculator (arbiter 12 #1-N) for receiving said clock skew sequences to determine the difference among the plurality of said clock skew sequences (col. 1, lines 44-46).

Regarding claims 5, 21 and 23, Gutnik discloses all limitation of the claim. Gutnik however, is silent regarding a timing jitter estimator for timing jitter sequences (patterns) of the clock signals and a clock skew calculator calculating timing differences in jitter. Dalal in a similar field of endeavor discloses a timing jitter estimator (fig. 6, element 745) for timing jitter sequences (patterns) of the clock signals and a clock skew calculator for receiving a plurality of timing jitter sequences (pattern) calculating timing differences in jitter (col. 4, lines 34-43; col. 5, lines 40-45). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a timing jitter estimator for timing jitter sequences (patterns) of the clock signals and a clock skew calculator calculating timing differences in jitter as taught by Dalal in the circuit of Gutnik because it can provide measurement samples indicative of signal level relative to the threshold.

Regarding claim 22, Gutnik discloses clock skew sequences includes a step of receiving said clock skew sequences and determining the difference among the

plurrality of the clock skew sequences, thereby estimating the probability of peak-to-peak clock skews (col. 6, lines 43-60; col. 10, lines 25-44).

Regarding claims 8 and 24, Gutnik discloses all limitation of the claim except a step of estimating timing errors among ideal clock edges of clock signals to estimate deterministic components of clock skews. Dalal in a similar field of endeavor discloses estimating timing errors among ideal clock edges of clock signals to estimate deterministic components of clock skews (col. 2, lines 31-42). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a step of estimating timing errors among ideal clock edges of clock signals to estimate deterministic components of clock skews as taught by Dalal in the circuit of Gutnik because it can allow accurate position and time of every edge to be measured in a statistical based measurement of sample signals.

As per claim 3, Gutnik shows limitation as disclosed above except determining an RMS value of data of the clock skew (jitter), a memory for storing a predetermined value, and a probability calculator for determining the peak-to-peak clock skews (jitter) among signals under test exceeding the predetermined value and RMS value. Dalal in a similar field of endeavor discloses an RMS value of data of the clock skew (jitter) (col. 4, lines 27-30; col. 7, lines 60-67); a memory (750) for storing a predetermined value (col. 7, lines 62-64); and a probability calculator for determining the peak-to-peak clock skews (jitter) among signals under test exceeding the predetermined value and RMS value (col. 8, lines 1-6). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a probability estimating means comprising

Art Unit: 2611

an RMS determination, a memory for storage results and probability calculation of peak-to-peak skews in signals as taught by Dalal in the system of Gutnik so that accurate sampling and estimation with the jitter measurement can be made with greater confidence and ease.

5. Claims 4, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al (USP 6,661,860) in view of Dalal (USP 6,661,836) and further in view of Voorakaranam et al "Low-cost Jitter Measurement Technique for Phase-Locked Loop", (Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, 2000).

Regarding claim 4, Gutnik and Dalal in combination disclose all limitation of the claim except an RMS detector, a peak-to-peak detector and a probability estimator. Voorakaranam in a similar field of endeavor discloses an RMS detector for determining an RMS value of data of the clock skew sequences supplied thereto (fig. 5, page 958, col. 1); a peak-to-peak detector for calculating maximum and minimum values of said clock skew sequence data to determine the peak-to-peak value (page 958, col. 2); and a probability calculator for determining the probability of the clock skews among the signals under test exceeding the peak-to-peak value based on said peak-to-peak value and said RMS value of the clock skew sequence data (page 958, col. 2; page 959, col. 1). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use RMS and peak-to-peak detection and jitter prediction (probability assessment) as taught by Voorakaranam in the combined system of Gutnik

Art Unit: 2611

and Dalal because it can provide a low cost detection and measurement of jitter for high speed signals.

Regarding claim 19, Gutnik and Dalal in combination disclose all limitation of the claim except determining an RMS value, storing a predetermined value in memory, and determining the probability of the peak-to-peak clock skew. Voorakaranam in a similar field of endeavor discloses an RMS detector for determining an RMS value of data of the clock skew sequences supplied thereto (fig. 5, page 958, col. 1); a peak-to-peak detector for calculating maximum and minimum values of said clock skew sequence data to determine the peak-to-peak value (page 958, col. 2); and a probability calculator for determining the probability of the clock skews among the signals under test exceeding the peak-to-peak value based on said peak-to-peak value and said RMS value of the clock skew sequence data (page 958, col. 2; page 959, col. 1). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use RMS and peak-to-peak detection and jitter prediction (probability assessment) as taught by Voorakaranam in the combined system of Gutnik and Dalal because it can provide a low cost detection and measurement of jitter for high speed signals.

Regarding claim 20, the steps claimed as method is nothing more than restating the function of the specific components of the apparatus claimed above and therefore, it would have been obvious to a person of ordinary skill in the art, considering the aforementioned rejection of claims 1, 17, to use the method in forming an apparatus because it can produce results as intended.

6. Claims 7, 13, 14 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al (USP 6,661,860) in view of Dalal (USP 6,661,836) and further in view of Godard (USP 4654861).

Regarding claim 7, Gutnik and Dalal combined disclose all limitations of the claim except clock skew estimator includes a frequency multiplier for receiving said timing jitter sequences and producing timing jitter sequences which are multiple of a frequency of said signals under test. Godard in a similar field of endeavor discloses a frequency multiplier for receiving said timing jitter sequences and producing timing jitter sequences which are multiple of a frequency of said signals under test (col. 6, lines 40-67; col. 7, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a multiplier to multiply a frequency of clock signals as taught by Godard in the combined system of Gutnik and Dalal because it can allow removal of residual jitter or noise from the output signal (col. 5, lines 42-56).

Regarding claim 13, Gutnik and Dalal combined show limitations as disclosed above. However, the combination is silent regarding clock skew (jitter) estimator includes an A/D converter for converting signals under test. Godard in a similar field of endeavor discloses (fig. 1, element 18), an ADC for converting signals under test to digital signals (col. 3, lines 25-56). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an ADC to convert the signals to digital signals as taught by Godard in the combined circuit of Gutnik and Dalal so as to provide proper transformation of signals in the jitter estimation process of signals.

Regarding claims 14 and 32, Gutnik and Dalal combined disclose all limitations to above claims however, the combination is silent regarding a step of conducting waveform clipping for the signals under test to remove amplitude modulation components in said signals under test thereby retaining only phase modulation components in said signals under test. Godard in a similar field of endeavor discloses limiting the signal to remove (clip) amplitude modulation in signals under test therefrom (col. 2, lines 18-19; col. 5, lines 50-56). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to remove amplitude modulation in signal as taught by Godard in the combined circuit of Gutnik and Dalal because it can provide reasonably accurate phase jitter measurement and estimation of signals.

7. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al (USP 6,661,860) in view of Dalal (USP 6,661,836) and further in view of Godard (USP 4654861).

Regarding claims 34, 35 Gutnik discloses a probability estimating apparatus (jitter estimation system and related techniques) for peak-to-peak values in clock skews (jitter) among a plurality of clock signals comprising:
a clock skew estimator (jitter estimation) for estimating clock skew sequences among the plurality of clock signals (SigA and SigB) under test (abstract; col. 5, lines 17-40; col. 6, lines 50-66). Gutnik however, does not explicitly disclose a probability estimator for determining a generation probability of the peak-to-peak values in the clock skews among the plurality of clock signals under test based on the clock skew sequences from

Art Unit: 2611

the clock skew estimator by applying Rayleigh distribution. Dalal in a similar field of endeavor discloses a probability estimator (creates a histogram that represents the probability density function of signal edge placement) for determining a generation probability of the peak-to-peak values in the clock skews among the plurality of signals (multiple repetitions of the signal) under test based on the clock skew sequences from the clock skew estimator (col. 2, lines 32-41; col. 3, lines 52-67; col. 4, lines 13-30; col. 5, lines 51-67). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use statistical estimation of applying Gaussian or Rayleigh distribution as taught by Dalal in the system of Gutnik because such estimation can provide instantaneous signal skew among interfering signal under test due to shift in frequency. The Gutnik and Dalal combination however, does not explicitly disclose clock skew estimator includes a frequency multiplier. Godard in a similar field of endeavor discloses a frequency multiplier for multiplying a frequency of clock signals under test (col. 6, lines 40-67; col. 7, lines 1-5). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a multiplier to multiply a frequency of clock signals as taught by Godard in the combined system of Gutnik and Dalal because it can allow removal of residual jitter or noise from the output signal (col. 5, lines 42-56).

The examiner notes that in the context of instant claims, signal fading as normally applied with mobile communication, is purely analytical and that Rayleigh distribution is well known in the art and applied to signals Gaussian in nature as noted in the attached

Art Unit: 2611

Text reference, pages 127-128, to Edward A. Lee and David G. Messerschmitt, as applied for estimating skew or deviation to estimates derived in Dalal.

As to claims 36 and 37, the steps claimed as method in nothing more than restating the function of the specific components of the apparatus as claimed above and therefore, it would have been obvious to a person of ordinary skill in the art to follow the method steps, considering the aforementioned rejection, to arrive at results as desired in jitter measurement using method steps for the apparatus claims 34-35.

Allowable Subject Matter

8. Claims 9-12, 15, 16, 25-31, 33 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents:

US Patent (6,922,452) to Sandberg.

US Patent (6,882,680) to Oleynik.

US Patent (5,402,443) to Wong.

US Patent (6,263,034) to Kanack et al.

US Patent (6,442,214) to Boleskei et al.

US Patent (5,757,652) to Blazo et al.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2611

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG.

October 30, 2006.


MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER